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IN THE CLAIMS:

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1           1. (Amended) A manufacturing method of a  
2 semiconductor integrated circuit device comprising a memory  
3 cell formed of a MISFET and a capacitor formed on a main  
4 surface of a semiconductor substrate, said method  
5 comprising the steps of:

6           (a) forming said MISFET on the main surface of said  
7 semiconductor substrate;

8           (b) forming an insulating film above said MISFET by  
9 the plasma CVD method at a temperature of 450°C to 700°C;

10          (c) forming a trench by etching said insulating film;

11          (d) depositing a silicon film on said insulating film  
12 and in said trench, and removing the silicon film on said  
13 insulating film to leave the silicon film only on an inner  
14 surface of said trench;

15          (e) forming a rugged surface silicon film on said  
16 silicon film on said inner surface of said trench to form a  
17 lower electrode of said capacitor on the inner wall of the  
18 trench; and

19          (f) forming a dielectric film on said rugged surface  
20 silicon film and on said insulating film and forming a  
21 plate electrode on said dielectric film.

1           2. (Amended) The manufacturing method of a  
2 semiconductor integrated circuit device according to claim  
A1 3 1, wherein said rugged surface silicon film is formed by  
4 crystal grains which are grown from crystal nucleuses of  
5 silicon deposited on said silicon film.

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Please cancel Claims 3, 7, 9, and 13 without prejudice.

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1           4. (Amended) The manufacturing method of a  
2 semiconductor integrated circuit device according to claim  
A2 3 1,  
4 wherein said semiconductor integrated circuit device  
5 has a first area in which said memory cell is formed and a  
6 second area in which a logic circuit is formed, and said  
7 manufacturing method of a semiconductor integrated circuit  
8 device comprises, before said step (b), the step of:  
9 (e) forming, in said second area in which a logic  
10 circuit is formed, an n channel MISFET and a p channel  
11 MISFET constituting said logic circuit, each of said n  
12 channel MISFET and said p channel MISFET comprising a gate  
13 electrode containing n type impurity and a gate electrode  
14 containing p type impurity, respectively.

1           5. (Amended) The manufacturing method of a  
2 semiconductor integrated circuit device according to claim  
3 1,  
4           wherein said plasma CVD method is a high-density  
5 plasma CVD.

Q2 1           6. (Amended) A manufacturing method of a  
2 semiconductor integrated circuit device comprising a memory  
3 cell including a MISFET and a capacitor formed on a main  
4 surface of a semiconductor substrate, said method  
5 comprising the steps of:

6           (a) forming said MISFET on the main surface of said  
7 semiconductor substrate;

8           (b) depositing a first insulating film above said  
9 MISFET at a first temperature;

10          (c) depositing a second insulating film on said first  
11 insulating film at a second temperature between 450°C and  
12 700°C that is higher than said first temperature;

13          (d) forming a trench by etching said first and second  
14 insulating films;

15          (e) depositing a silicon film on said second  
16 insulating film and in said trench, and removing the

17 silicon film on said second insulating film to leave the  
18 silicon film only on an inner surface of said trench;  
19 (f) forming a rugged surface silicon film on said  
20 silicon film on said inner surface of said trench to form a  
Q2 21 lower electrode of said capacitor on the inner wall of the  
22 trench; and  
23 (g) forming a dielectric film on said rugged surface  
24 silicon film and on said second insulating film and forming  
25 a plate electrode on said dielectric film.

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1 10. (Amended) The manufacturing method of a  
2 semiconductor integrated circuit device according to claim  
3 6,  
4 wherein said semiconductor integrated circuit device  
Q3 5 has a first area in which said memory cell is formed and a  
6 second area in which a logic circuit is formed, and said  
7 manufacturing method of a semiconductor integrated circuit  
8 device comprises, before said step (b), the step of:  
9 (h) forming, in said second area in which a logic  
10 circuit is formed, an n channel MISFET and a p channel  
11 MISFET constituting said logic circuit, each of said n  
12 channel MISFET and said p channel MISFET comprising a gate

13 electrode containing n type impurity and a gate electrode  
14 containing p type impurity, respectively.

1 11. (Amended) A manufacturing method of a  
2 semiconductor integrated circuit device, comprising the  
3 steps of:

4 (a) forming a MISFET on a main surface of a  
5 semiconductor substrate;

Q3 6 (b) forming an insulating film containing impurity  
7 above said MISFET by a high density plasma CVD method at a  
8 temperature of 450°C to 700°C;

9 (c) forming a trench by etching said insulating film;

10 (d) depositing a silicon film on said insulating film  
11 and in said trench, and removing the silicon film on said  
12 insulating film to leave the silicon film only on an inner  
13 surface of said trench;

14 (e) forming a rugged surface silicon film on said  
15 silicon film on said inner surface of said trench to form a  
16 lower electrode of a capacitor on the inner wall of the  
17 trench; and

18 (f) forming a dielectric film on said rugged surface  
19 silicon film and on said insulating film and forming a  
20 plate electrode on said dielectric film.

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1           14. (Amended) A manufacturing method of a  
2 semiconductor integrated circuit device, comprising the  
3 steps of:  
4           (a) forming a MISFET on a main surface of a  
5 semiconductor substrate;  
6           (b) depositing a first insulating film above said  
7 MISFET at a first temperature;  
8           (c) planarizing a surface of said first insulating  
9 film;  
10           (d) forming a second insulating film containing  
11 impurity on said first insulating film at a second  
12 temperature higher than said first temperature;  
13           (e) forming a trench by etching said first and second  
14 insulating films;  
15           (f) depositing a silicon film on said second  
16 insulating film and in said trench, and removing the  
17 silicon film on said second insulating film to leave the  
18 silicon film only on an inner surface of said trench;  
19           (g) forming a rugged surface silicon film on said  
20 silicon film on said inner surface of said trench to form a  
21 lower electrode of a capacitor on the inner wall of the  
22 trench; and